WHAT IS CLAIMED IS:

1. A ring oscillator, comprising:

a feedback input terminal;

a circuit output terminal for generating an oscillator output signal; and

a positive feedback loop between said circuit output terminal and said feedback input terminal,

said positive feedback loop including a plurality of delaying stages connected in cascade, and a transfer gate coupled to each of said plurality of delaying stages, each of said transfer gates including a pair of transistors of the first and second conductivity types connected in parallel, said transistors of the first conductivity type being controlled by a first control signal, said transistors of the second conductivity type being controlled by a second control signal.

2. The ring oscillator as claimed in claim 1, wherein said positive feedback loop includes, as said plurality of delaying stages, an odd number of delaying inverting stages, each of said delaying inverting stages including a CMOS inverter, and wherein said pair of transistors of each transfer gate are p-channel and n-channel transistors, respectively, and wherein said ring oscillator is operable during a first mode when said p-channel transistors are ON and said n-channel transistors are OFF, during a second mode when said p-channel transistors are OFF and said n-channel transistors are ON, and during a third mode when said p-channel and n-channel transistors are both ON.

3. The ring oscillator as claimed in claim 1, wherein said positive feedback loop includes an NAND input stage, wherein said positive feedback loop includes, as said plurality of delaying stages, an even number of delaying inverting stages following said NAND input stage, each of said delaying inverting stages including a CMOS inverter, and wherein said first and second conductivity type transistors are

p-channel and n-channel transistors, respectively, and wherein said ring oscillator is operable during a first mode when said p-channel transistors are ON and said n-channel transistors are OFF, during a second mode when said p-channel transistors are OFF and said n-channel transistors are ON, and during a third mode when said p-channel and n-channel transistors are both ON.

4. The ring oscillator as claimed in claim 2, wherein said first control signal has two levels, and said second control signal has two levels, and further comprising a control circuit in communication with gates of said p-channel transistors and with gates of said n-channel transistors for shifting said first control signal between said two levels thereof and said second control signal between said two levels thereof.

5. The ring oscillator as claimed in claim 3, wherein said first control signal has two levels, and said second control signal has two levels, and further comprising a first terminal connected to gates of said p-channel transistors and a second terminal connected to gates of said n-channel transistors, said first and second terminals being communicable with a control circuit for shifting said first control signal between said two levels thereof and said second control signal between said two levels thereof.

6. The ring oscillator as claimed in claim 1, further comprising a divider in communication with said circuit output terminal and operable to receive said oscillator output signal.

7. The ring oscillator as claimed in claim 2, further comprising a divider in communication with said circuit output terminal and operable to receive said oscillator output signal.

8. The ring oscillator as claimed in claim 3, further comprising a divider in communication with said circuit output terminal and operable to receive said oscillator output signal.

9. The ring oscillator circuit as claimed in claim 4, further comprising a divider in communication with said circuit output terminal and operable to receive said oscillator output signal.

10. The ring oscillator circuit as claimed in claim 5, further comprising a divider in communication with said circuit output terminal and operable to receive said oscillator output signal.

11. A semiconductor integrated circuit comprising said ring oscillator as claimed in claim 1.

12. The semiconductor integrated circuit as claimed in claim 11, wherein said positive feedback loop includes, as said plurality of delaying stages, an odd number of delaying inverting stages, each of said delaying inverting stages including a CMOS inverter, and wherein said pair of transistors of each transfer gate are p-channel and n-channel transistors, respectively, and wherein said ring oscillator is operable during a first mode when said p-channel transistors are ON and said n-channel transistors are OFF, during a second mode when said p-channel transistors are OFF and said n-channel transistors are ON, and during a third mode when said p-channel and n-channel transistors are both ON.

13. The semiconductor integrated circuit as claimed in claim 11, wherein said positive feedback loop includes an NAND input stage, wherein said positive feedback loop includes, as said plurality of delaying stages, an even number of delaying inverting stages following said NAND input stage, each of said delaying inverting stages including a CMOS inverter, and wherein said first and second conductivity type transistors are p-channel and n-channel transistors, respectively, and wherein said ring oscillator is operable during a first mode when said p-channel transistors are ON and said n-channel transistors are OFF, during a second mode when said p-channel transistors are OFF and said n-channel transistors are ON, and during

a third mode when said p-channel and n-channel transistors are both ON.

14. The semiconductor integrated circuit as claimed in claim 12, wherein said first control signal has two levels, and said second control signal has two levels, and further comprising a first terminal connected to gates of said p-channel transistors and a second terminal connected to gates of said n-channel transistors, said first and second terminals being communicable with a control circuit for shifting said first control signal between said two levels thereof and said second control signal between said two levels thereof.

15. The semiconductor integrated circuit as claimed in claim 13, wherein said first control signal has two levels, and said second control signal has two levels, and further comprising a first terminal connected to gates of said p-channel transistors and a second terminal connected to gates of said n-channel transistors, said first and second terminals being communicable with a control circuit for shifting said first control signal between said two levels thereof and said second control signal between said two levels thereof.

16. The semiconductor integrated circuit as claimed in claim 11, further comprising a divider in communication with said circuit output terminal and operable to receive said oscillator output signal.

17. The semiconductor integrated circuit as claimed in claim 12, further comprising a divider in communication with said circuit output terminal and operable to receive said oscillator output signal.

18. The semiconductor integrated circuit as claimed in claim 13, further comprising a divider in communication with said circuit output terminal and operable to receive said oscillator output signal.

19. The semiconductor integrated circuit as claimed in claim 14,

further comprising a divider in communication with said circuit output terminal and operable to receive said oscillator output signal.

20. The semiconductor integrated circuit as claimed in claim 15, further comprising a divider in communication with said circuit output terminal and operable to receive said oscillator output signal.

21. The ring oscillator as claimed in claim 2, wherein each of said transfer gates is coupled to the input of one of said CMOS inverters that follow said transfer gate.

22. The ring oscillator as claimed in claim 3, wherein each of said transfer gates is coupled to the input of one of said CMOS inverters that follow said transfer gate, and wherein said NAND input stage is coupled to one of said transfer gates that follow.

23. A test method for verifying fabrication of transistors in an integrated circuit, comprising:

providing a ring oscillator on a die under test during fabrication of said die, said ring oscillator including a plurality of delaying stages connected in cascade, and a transfer gate coupled to each of said plurality of delaying stages, each of said transfer gates including a pair of transistors of the first and second conductivity types connected in parallel, said transistors of the first conductivity type and said transistors of the second conductivity type being fabricated by same processes as transistors of the first conductivity type and transistors of the second conductivity type constituting an integrated circuit on said die;

measuring a first period of said ring oscillator by operating said ring oscillator to provide a first oscillator output signal during a first mode when said transistors of the first conductivity type of each of said transfer gates are ON and said transistors of the second conductivity type of each of said transfer gates are OFF;

measuring a second period of said ring oscillator by operating

said ring oscillator to provide a second oscillator output signal during a second mode when said transistors of the first conductivity type of each of said transfer gates are OFF and said transistors of the second conductivity type of each of said transfer gates are ON;

measuring a third period of said ring oscillator by operating said ring oscillator to provide a third oscillator output signal during a third mode when said transistors of the first conductivity type of each of said transfer gates are ON and said transistors of the second conductivity type of each of said transfer gates are ON; and

analyzing said first, second and third periods for decision making on whether said integrated circuit on said die meets preselected specification.

24. The test method as claimed in claim 23, wherein said step of analyzing includes the steps of:

comparing said first period with a first preselected specification;

comparing said second period with a second preselected specification; and

comparing said third period with a third preselected specification.

25. The test method as claimed in claim 23, wherein the total number of said plurality of delaying stages is odd, wherein each of said delaying stages includes a CMOS inverter, and wherein said pair of transistors of each transfer gate are p-channel and n-channel transistors, respectively.

26. The test method as claimed in claim 23, wherein said ring oscillator includes an NAND input stage, wherein the total number of said plurality of delaying stages is even, and wherein each of said delaying stages includes a CMOS inverter, and wherein said first and second conductivity type transistors are p-channel and n-channel transistors, respectively.

27. A test apparatus for verifying fabrication of transistors in an integrated circuit, comprising:

a ring oscillator provided on a die under test during fabrication of said die, said ring oscillator including a plurality of delaying stages connected in cascade, and a transfer gate coupled to each of said plurality of delaying stages, each of said transfer gates including a pair of transistors of the first and second conductivity types connected in parallel, said transistors of the first conductivity type and said transistors of the second conductivity type being fabricated by same processes as transistors of the first conductivity type and transistors of the second conductivity type constituting an integrated circuit on said die;

circuitry operable for measuring

a first period of said ring oscillator by operating said ring oscillator to provide a first oscillator output signal during a first mode when said transistors of the first conductivity type of each of said transfer gates are ON and said transistors of the second conductivity type of each of said transfer gates are OFF,

a second period of said ring oscillator by operating said ring oscillator to provide a second oscillator output signal during a second mode when said transistors of the first conductivity type of each of said transfer gates are OFF and said transistors of the second conductivity type of each of said transfer gates are ON, and

a third period of said ring oscillator by operating said ring oscillator to provide a third oscillator output signal during a third mode when said transistors of the first conductivity type of each of said transfer gates are ON and said transistors of the second conductivity type of each of said transfer gates are ON; and

circuitry operable for analyzing said first, second and third periods for decision making on whether said integrated circuit on said die meets preselected specification.

28. The test apparatus as claimed in claim 27, wherein said circuitry operable for analyzing includes:

circuitry operable for comparing said first period with a first preselected specification;

circuitry operable for comparing said second period with a second preselected specification; and

circuitry operable for comparing said third period with a third preselected specification.

29. A computer program product embodied in a storage media, the computer program product including a program of instructions for performing:

measuring a first period of a ring oscillator for a die under test,

wherein said ring oscillator is provided on said die during fabrication of said die, said ring oscillator including a plurality of delaying stages connected in cascade, and a transfer gate coupled to each of said plurality of delaying stages, each of said transfer gates including a pair of transistors of the first and second conductivity types connected in parallel, said transistors of the first conductivity type and said transistors of the second conductivity type being fabricated by same processes as transistors of the first conductivity type and transistors of the second conductivity type constituting an integrated circuit on said die,

said step of measuring said first period being carried out by operating said ring oscillator to provide a first oscillator output signal during a first mode when said transistors of the first conductivity type of each of said transfer gates are ON and said transistors of the second conductivity type of each of said transfer gates are OFF;

measuring a second period of said ring oscillator by operating said ring oscillator to provide a second oscillator output signal during a second mode when said transistors of the first conductivity type of each of said transfer gates are OFF and said transistors of the second conductivity type of each of said transfer gates are ON;

measuring a third period of said ring oscillator by operating said ring oscillator to provide a third oscillator output signal during a third mode when said transistors of the first conductivity type of each of

said transfer gates are ON and said transistors of the second conductivity type of each of said transfer gates are ON; and

analyzing said first, second and third periods for decision making on whether said integrated circuit on said die meets preselected specification.

30. The computer program product as claimed in claim 29, wherein said step of analyzing includes:

comparing said first period with a first preselected specification;

comparing said second period with a second preselected specification; and

comparing said third period with a third preselected specification.